REMARKS

This Amendment responds to the Final Office Action mailed July 11, 2008, in the above-identified application. The amendments do not raise new issues or require extensive consideration. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1-8, 25 and 27 were previously pending in the application. By this Amendment, claim 1 is amended and claim 27 is canceled without prejudice or disclaimer. Accordingly, claims 1-8 and 25 are currently pending, with claim 1 being the sole independent claim.

The Examiner has rejected claims 1-3, 7, 25 and 27 under 35 U.S.C. §103(a) as unpatentable over Heath et al. (U.S. 4,901,234) in view of Dowling (U.S. 6,163,836). Claims 4-6 and 8 are rejected under 35 U.S.C. §103(a) as unpatentable over Heath et al. in view of Dowling, further in view of Bowes et al. (U.S. 5,655,151). The rejections are respectfully traversed for the following reasons.

Heath discloses a computer system in which peripherals greater in number than the number of DMA channels provided in the system can all have DMA access. Some of the DMA channels are dedicated to certain ones of the peripherals, while others, termed "programmable" DMA channels, are shared by remaining ones of the peripherals (Abstract). A DMA controller 12 is coupled to a system bus 26 and to a family bus 25 (FIG. 1). The details of DMA controller 12 are shown in FIG. 6 of Heath.

Dowling discloses a programmable address arithmetic unit and method for use on microprocessors, microcontrollers and digital signal processors (Abstract). FIG. 2 of Dowling shows a programmable address arithmetic unit (AAU) 212 and a fixed function AAU 106. An output of one of the AAUs is selected by a MUX 203 and provided to a register set 102. A MUX 122 selects *a single address* to be provided to data memory 120 at any given time. FIG. 6 of Dowling discloses a very long instruction word DSP 600 with a first programmable AAU 617 and a second programmable AAU 619 (col. 17, lines 20-23). Addresses to a data memory 658 are provided by a first address multiplexer 650 and a second address multiplexer 652 (col. 17, lines 33-35). Dowling does not disclose a DMA controller.

Claim 1 has been amended to incorporate the limitations of claim 27 and recites that the multiplexer supplies the first and second current memory addresses to the first and second memory pipelines at the same time. It is submitted that the amendment does not raise new issues because amended claim 1 corresponds to previous claim 27. Accordingly, entry of the amendment is respectfully requested.

The present invention relates to a DMA controller, shown by way of example only in FIG. 2 of the present application, which includes independent memory pipelines configured to operate in parallel at the same time such that neither memory pipeline needs to wait for resources. A DMA controller as claimed is not disclosed or even remotely suggested by the combination of Heath and Dowling.

The Examiner acknowledges that Heath fails to disclose a controller having first and second address computation units for generating addresses at the same time to permit DMA transfer of data, but asserts that Dowling cures this deficiency. Applicants submit that amended claim 1 is clearly distinguished over Heath in view of Dowling.

First, Dowling discloses memory addressing in connection with program execution by a processor rather than a DMA controller. Applicants continue to maintain that the skilled person would not refer to the teachings of Dowling relating to program execution in order to modify the DMA controller of Heath.

Second, the address arithmetic units 212 and 106 shown in FIG. 2 of Dowling provide only a single address to memory 120 at any time. Address multiplexer 122 provides an address to data memory 120 from register set 102 or from program bus 101, but not two data addresses at the same time. By contrast, Applicant's amended claim 1 recites *a multiplexer that supplies the first and second current memory addresses to the first and second memory pipelines at the same time*. See, for example, MUX 124 in FIG. 2 of the present application. FIG. 2 of Dowling and the corresponding description do not disclose or suggest a multiplexer as recited by claim 1 and do not disclose or suggest first and second address computation units which permit DMA transfer of data from one memory space to another memory space on the first and second memory access buses, as required by claim 1.

Regarding claim 27, the Examiner asserts that Heath as modified by Dowling teaches a DMA controller wherein the multiplexer supplies the first and second current memory addresses to the first and second memory pipelines at the same time, with reference to column 5, lines 13-20. Applicant must respectfully disagree. It is unclear whether the passage cited in the rejection of claim 27 refers to Heath or Dowling. However neither reference contains a teaching of the claim limitation. Dowling at column 5, lines 13-20 teaches a processor that uses a dispatch circuit to provide instructions to many instruction units in a single instruction cycle, and a memory queue configured to queue memory requests from a programmable AAU. Clearly, this is very different from teaching a multiplexer that supplies first and second current memory addresses to first and second memory pipelines at the same time. Heath at column 5, lines 13-20 describes that one compare logic is provided for each of the programmable physical DMA channels in the system and that one compare logic is provided for each of the fixed channels. Again, this is very different from teaching a multiplexer that supplies first and second current memory addresses to the first and second memory pipelines at the same time, as required by amended claim 1.

As noted above, FIG. 6 of Dowling shows a first programmable AAU 617 and a second programmable AAU 619 connected to data memory 658 through address multiplexers 650 and 652, respectively. However, FIG. 6 of Dowling and the accompanying description do not disclose or suggest first and second address computation units which generate addresses at the same time to permit *DMA transfer of data from one memory space to another memory space* on first and second memory access buses, as required by claim 1. Instead, the accessed data words from memory 658 are loaded into registers in register files 632, 634 for operation by the functional units (Col. 17, lines 61-66). Again, Dowling does not disclose or suggest a DMA controller.

For at least these reasons, amended claim 1 is clearly and patentably distinguished over Heath in view of Dowling, and withdrawal of the rejection is respectfully requested.

Claims 2-8 and 25 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Based upon the above discussion, entry of the Amendment and allowance of the application are respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, the Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed, or which should have been filed herewith to our Deposit Account No. 23/2825, under Docket No. A0312.70515US00.

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Respectfully submitted,

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